

# The PHENIX Data Acquisition System

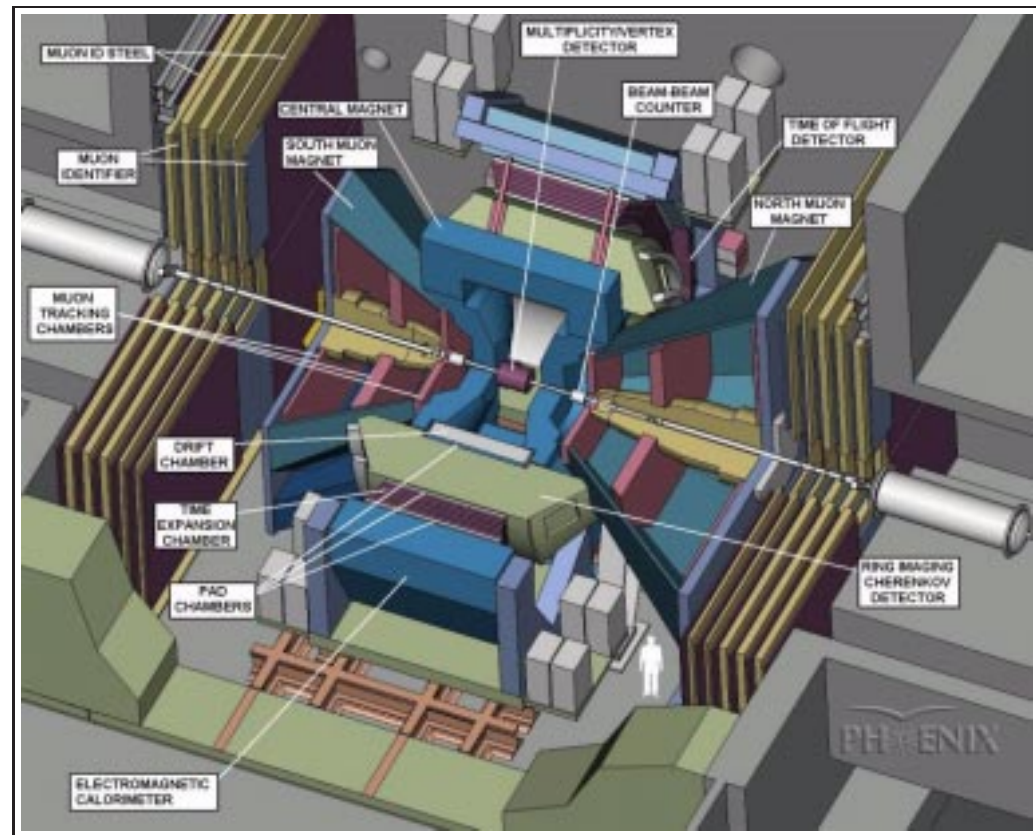
Brian A Cole

Columbia University Nevis Labs

for the PHENIX Collaboration

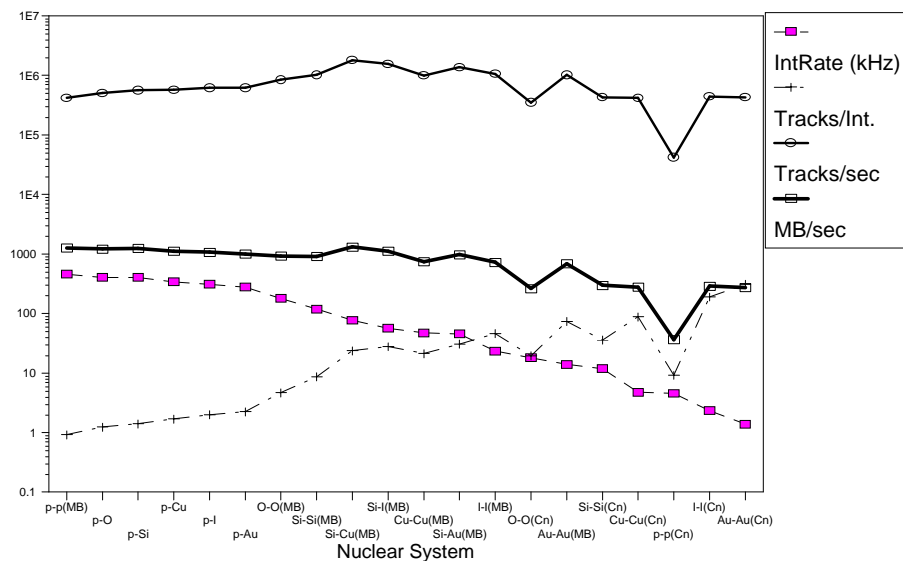
## Outline

1. Design Requirements
2. Overview
3. Data Collection Modules
4. Event Builder
5. Status Report



## PHENIX DAQ Requirements

Expected event/data rates at  
10× RHIC design Luminosity  
(W. Zajc)



### Physics Considerations

- PHENIX is designed for high rate, rare processes.
- Physics goals include probes at  $\sim 100$  to  $< 10^{-6}$  per collision.
- Large dynamic range in event size, event rate.

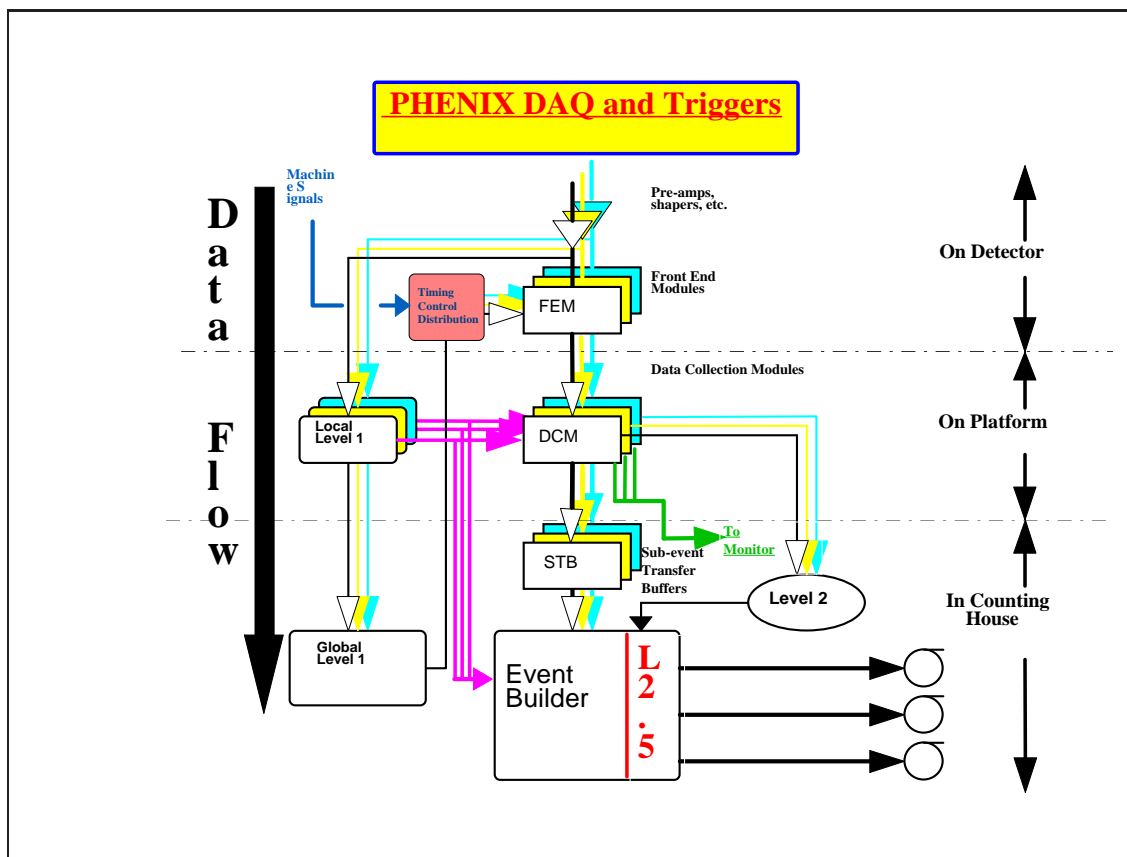
### Architecture

- Collider experiment  $\rightarrow$  pipelined system.
- Multi-level collapse/trigger  $\rightarrow$  data-driven.
- No “simple” triggers  $\rightarrow$  build event, then trigger.

### Design Parameters

- Front-end conversion time =  $40 \mu s$   
 $\rightarrow$  Maximum level-1 trigger rate 25 kHz.
- Initially will run with  $80 \mu s$  conversion time  
 $\rightarrow$  Maximum level-1 trigger rate 12.5 kHz.
- Design event-builder bandwidth = 2 Gbyte/s.
- “Baseline” bandwidth = 500 Mbyte/s.

## DAQ System Overview

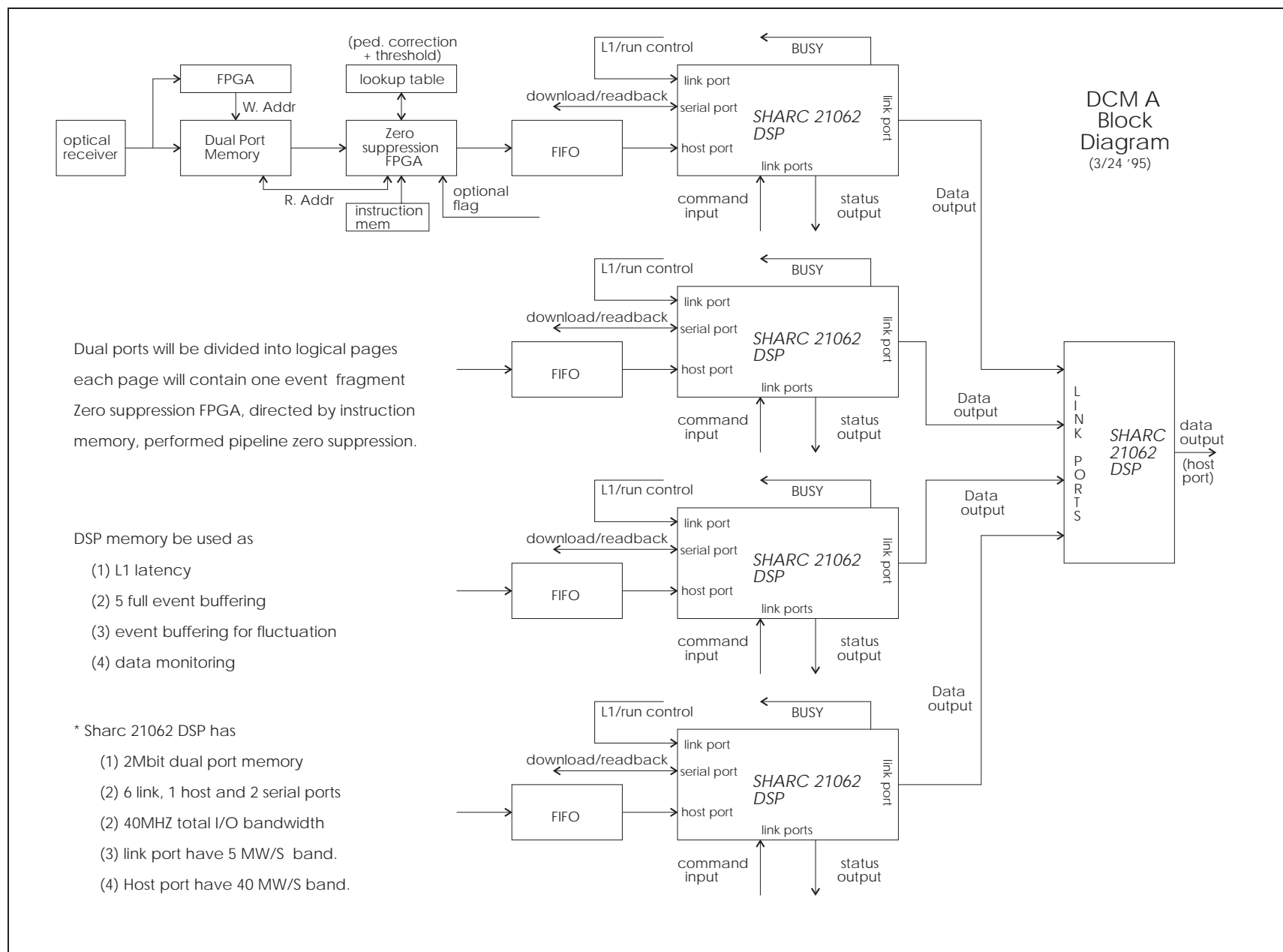


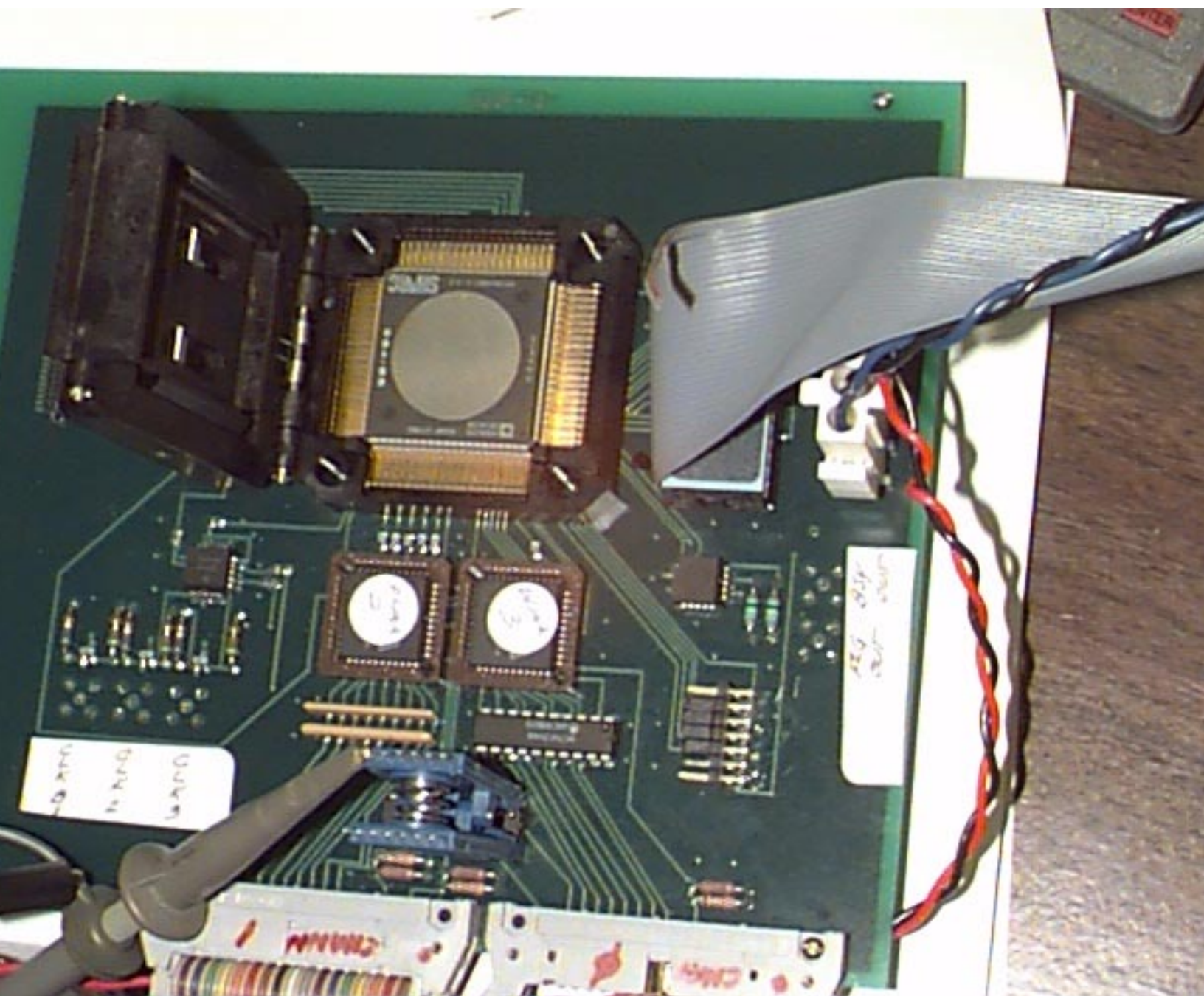
## PHENIX DAQ Dataflow

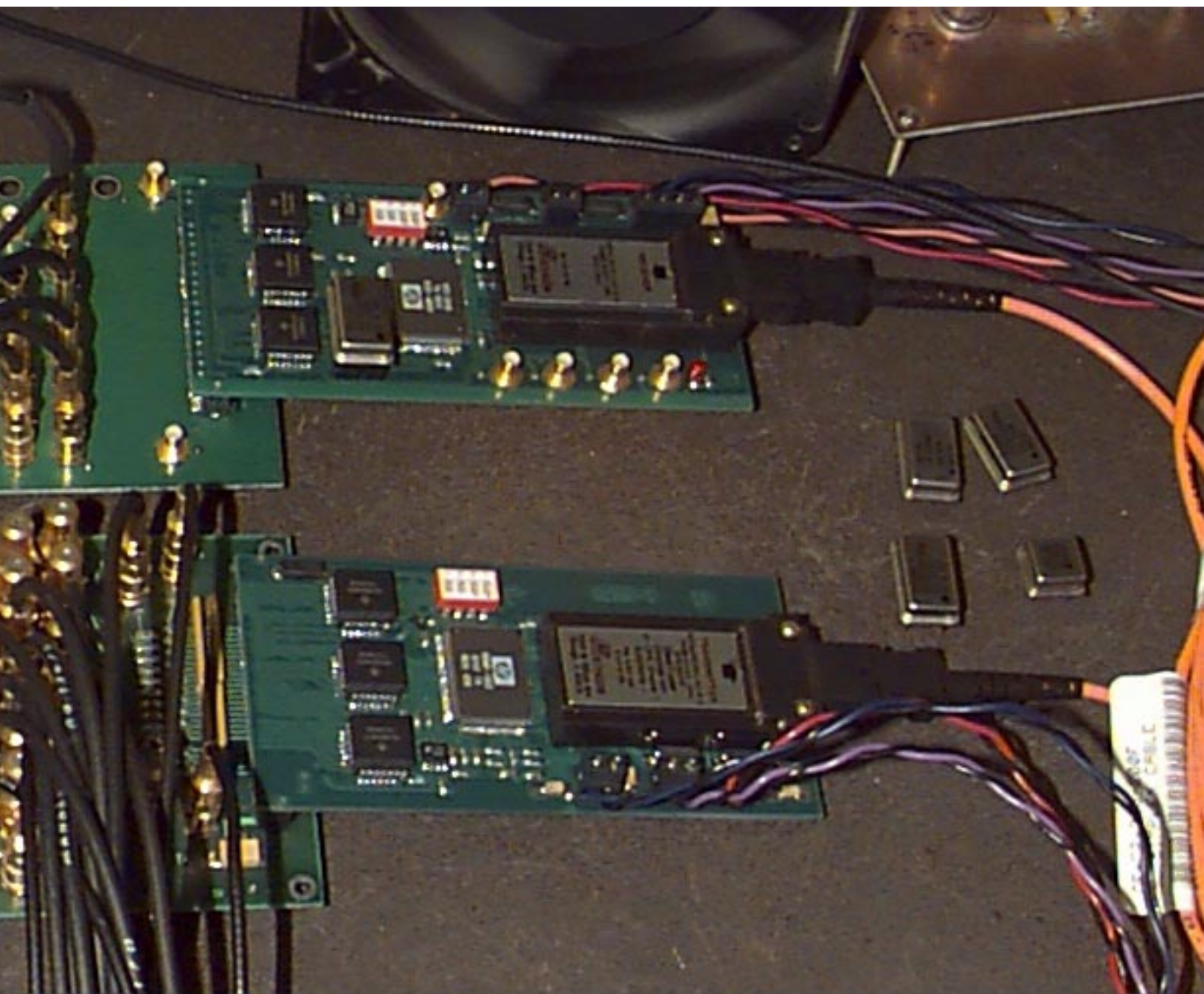
1. "Signals" buffered in analog/digital memory until Level-1 Decision.
2. Data transferred to DCM in fixed format.
3. Zero-suppression performed at DCM "input".
4. Pedestal subtraction, calibration applied in DCM.
5. Data transferred to SEB.
6. SEB's collapse and buffer data.
7. Event-builder creates complete events, runs Level-2.5 trigger.
8. Accepted events transferred to ONCS.

(See John Haggerty's talk re: interfaces)

## The PHENIX Data Collection Module





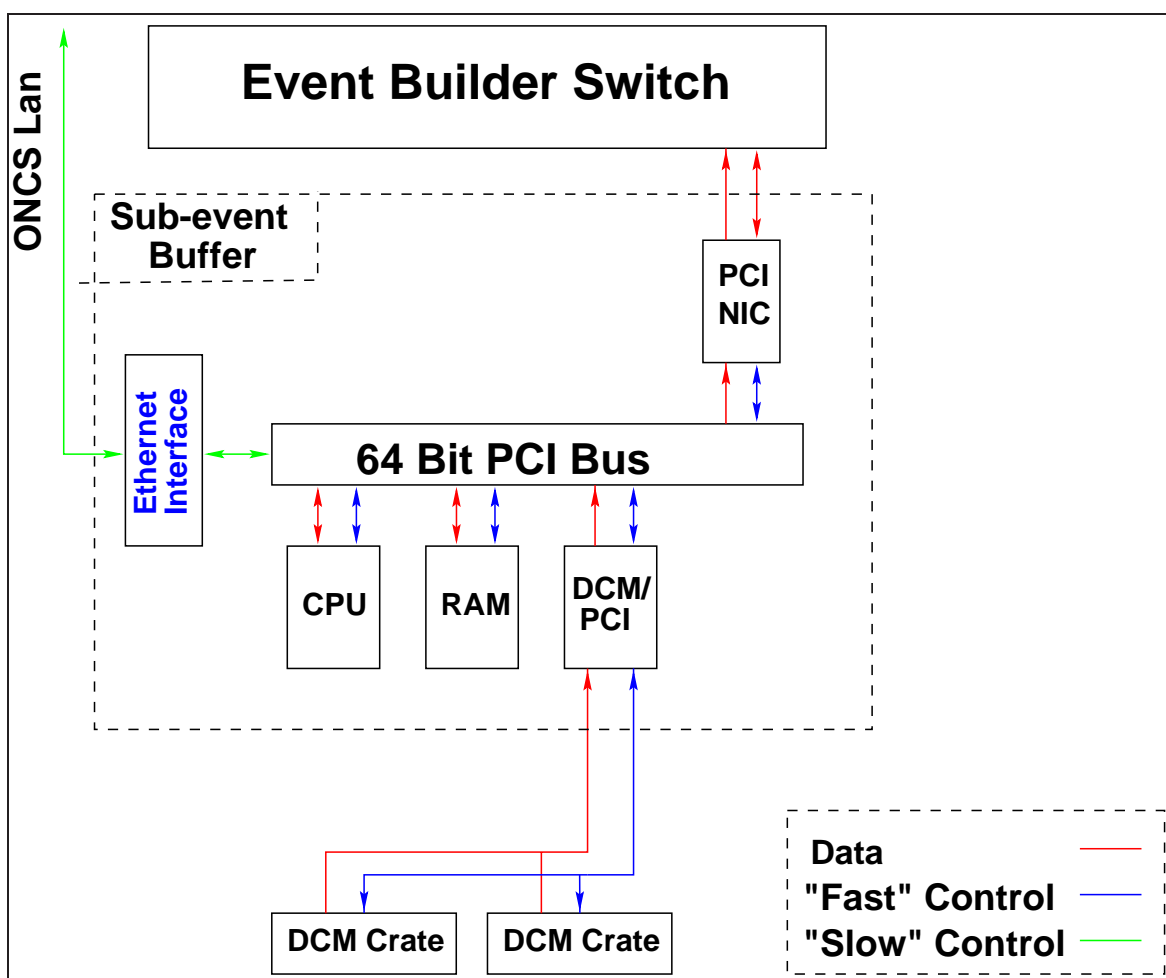




## The PHENIX Event Builder – Sub-event Buffer (SEB)

### SEB Design Guidelines:

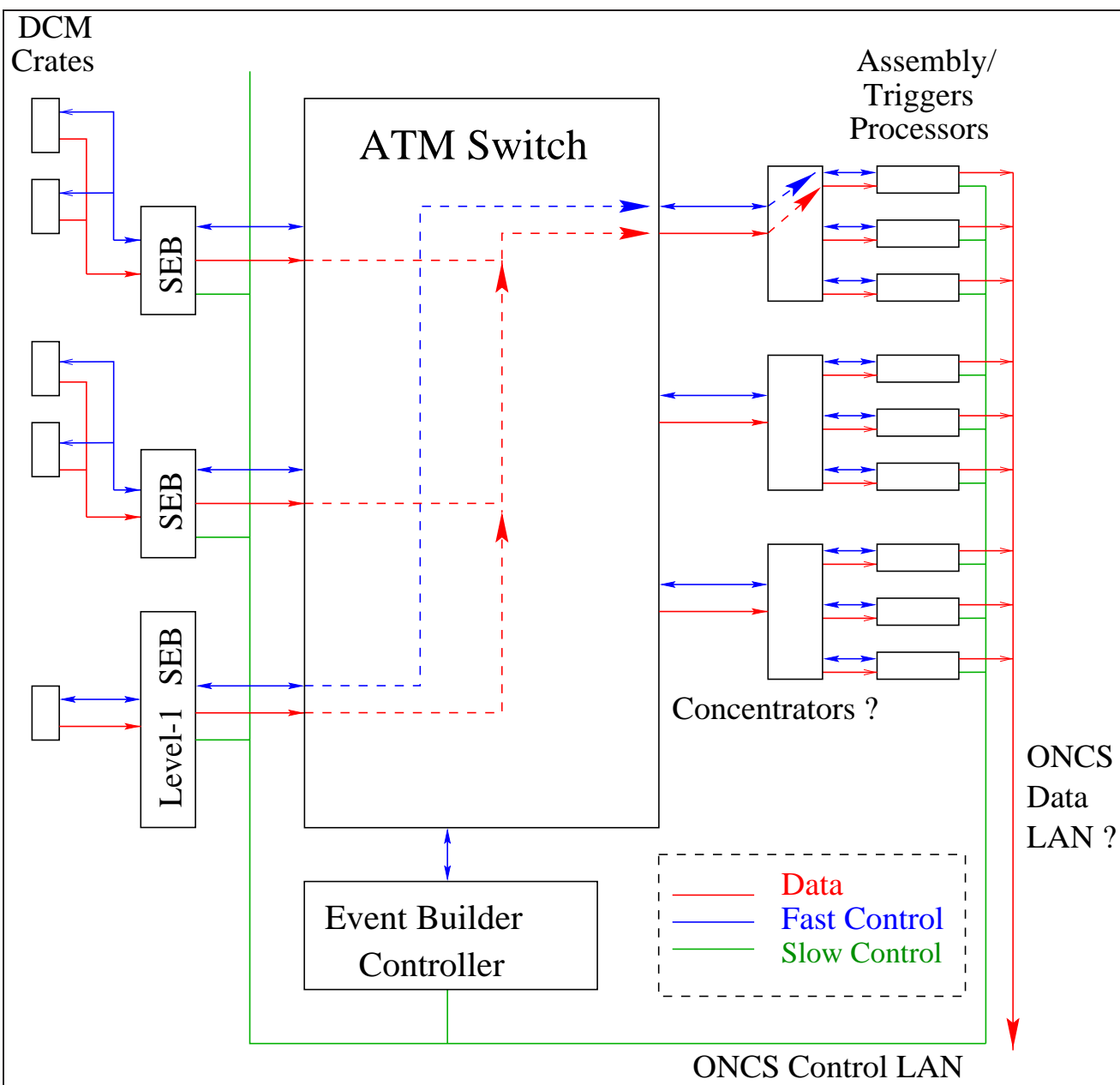
- Use commodity commercial processor → Intel/Alpha/?
- Use standard commercial bus → PCI.
- Use common operating system → NT/VXWorks/LynxOS.
- Use commercial ATM (OC-3) interface card → not yet specified.
- Use commercial receiver card for DCM data (possibly with personality card) → not yet specified.



## The PHENIX Event Builder

### Major Functions

- Receive data from DCM's into sub-event buffers (SEB's).
- Switch fragments of event to Assembly Trigger Processors (ATP's).
- Assemble event. Run trigger algorithm.
- Pass complete, trigger-selected events to ONCS.



## DAQ System Development Status

### Data Collection Modules

1. Functional specs/logical design now mature.
2. All individual components bench tested.
3. Complete Prototype design will be finished imminently.
4. Prototype available within 2-3 months.

### Sub-event Buffers

1. Prototype system chosen, purchased for SEB.
2. DCM  $\rightarrow$  PCI interface choice imminent.
3. Will likely try two ATM NIC's, IDT + Fore (?)
4. Prototype SEB must be complete for Fall Sector test.

### ATM Switch

1. Top candidate  $\rightarrow$  FORE ASX1000 (10 Gbit/s, 64-port).
2. Matching of data rates from SEB's to switch demonstrated for Au+Au central at  $10\times$  design luminosity.
3. Will likely be purchased within 1-2 months.

### Assembly trigger processors

1. Hardware will be similar to SEB.
2. Same ATM NIC+Driver as in SEB.
3. Software design in progress.